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Applicant respectfully disagrees with the Examiner's assertions and conclusion. Applicant's invention is directed toward a semiconductor device precursor having a polycrystalline silicon layer with a smooth morphology while simultaneously being free of metal contaminants. An embodiment of the present invention involves a layer of silicon dioxide (Fig. 1; page 8, lines 13-20), hydrogen ions implanted into the layer of silicon dioxide by plasma source ion implantation (page 8, lines 25-28 and page 9, lines 1-28), and then a layer of polycrystalline silicon is formed on the layer of the treated silicon dioxide (page 9, lines 2-7). The hydrogen ions are implanted into the silicon dioxide by applying a high voltage pulse to the semiconductor substrate. The layer of polycrystalline silicon formed over the treated silicon dioxide has a smooth morphology (page 10, lines 8-18). By implanting the hydrogen ions into the silicon dioxide layer using the target object itself to accelerate the hydrogen ions toward the target object, the possibility of contamination of the target object is reduced (page 10, lines 21-24).

As described in the specification, in the Background section at pages 1-2, a need exists for a process by which silicon dioxide films can be pretreated to ensure that a subsequently deposited polycrystalline silicon film will be provided with a smooth morphology but without contamination (page 2, lines 24-27). In the prior art, silicon dioxide films are pretreated with hydrogen ions to prepare the surface of the silicon dioxide film for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film (page 1, lines 12-14). The silicon dioxide is pretreated by a hydrogen ion beam bombardment by a Kaufman ion source (page 1, lines 15-16). During ion implantation process using a Kaufman ion source, metal from the metal grid sputters off the grid and becomes implanted in the target object causing the target object to become contaminated (page 1, lines 19-21). As the size of devices on the target object decreases, the effect of damage caused by sputtered metal from the metal grid increases (page 1, lines 22-24).

Also described in the specification, Background section at pages 1-2, plasma source ion implantation (PSII) has been used to dope materials by implanting ions into a target at energies that are high enough to bury the ions below the target's surface (page

2, lines 1-4). An ionized plasma is formed around the target in an enclosed chamber, then a high voltage pulse is applied to the target driving the ions from the plasma into the surfaces of the target simultaneously without manipulating the target (page 2, lines 5-9).

Examples of two different approaches to using PSII are provided in specification at page 2, lines 10-24. One example is a method and apparatus for using PSII that can be performed on complex, three-dimensional objects formed of a variety of materials such as: pure metals, alloys, semi-conductors, ceramics, and organic polymers (page 2, lines 8-11). The second example of using PSII is directed to an apparatus which uses a pair of power supplies and short ionization negative pulses applied to the cathode underlying the target in conjunction with or followed by short ionization pulses applied to a second cathode which is facing toward the primary target to provide neutralizing electrons (page 2, 15-22).

The techniques explained above, including the two different approaches of using PSII, possess deficiencies, namely the techniques cannot provide a smooth morphology of the polycrystalline silicon while simultaneously being free of metal contaminants. An embodiment of the present invention teaches a third approach to using PSII to cure the deficiencies found in the previous uses of PSII, including the deficiencies found in the above two approaches, by providing a precursor that has a smooth morphology on the layer of polycrystalline silicon while simultaneously having a layer of silicon dioxide free of metal contaminants. This is accomplished by implanting hydrogen ions into the silicon dioxide layer by PSII. No prior art teaches, suggests, or provides motivation to one skilled in the art to create such a semiconductor device precursor.

Applicant submits that it would not have been obvious to one of ordinary skill in the art to use PSII to implant the hydrogen ions because the prior art does not teach or suggest using the same methods to obtain the same desired result as the claimed invention. The present invention teaches implanting plasma hydrogen ions uniformly on a silicon dioxide surface to provide a smooth surface morphology for a subsequently

deposited polysilicon layer by decreasing surface contamination, specifically metal contamination. The prior art teachings do not teach or suggest the claimed invention.

The Examiner states that the prior art teaches a Kaufman source to implant hydrogen ions into a surface of silicon dioxide to form a smooth surface. As applicant teaches in his specification, using a Kaufman source can cause surface contamination which interferes with the morphology of a subsequently deposited layer. The Examiner concedes that the prior art does not teach implanting hydrogen ions using plasma source ion implantation. Thus, the prior art suffers from the shortcoming of having metal contaminants with no motivation provided to one skilled in the art to rectify this shortcoming.

Next, the Examiner asserts that the prior art teaches using PSII without a metal grid to dope various materials. The prior art described in the specification contains a generalized teaching of plasma source ion implantation, however, the prior art does not address using plasma source ion implantation in order to provide smooth surface morphology. Furthermore, the prior art does not teach or suggest the specific materials and combinations recited in claim 9. Rather, the specification contains a generalized teaching of PSII with examples of two different approaches to using PSII, explained above (page 2, lines 1-24). The advantages described for PSII do not pertain to and are not even applicable to the Kaufman method, which is unconcerned about surface hardness.

The Examiner has attempted to combine unrelated prior art teachings in an effort to arrive at the claimed invention. The mere fact that the references can be combined does not render the resultant combination obvious unless that prior art also suggests the desirability of the combination. *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990) and MPEP §2143.01; *See also In re Lee*, 61 USPQ2d 1430. The desirability of the combination is not suggested in the prior art, therefore, the Examiner's proposed combination is based on prohibited hindsight.

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The prior art referenced by the Examiner, strictly teaches the use of the Kaufman source with hydrogen ions in order to provide for a thinner smoother polycrystalline silicon film. There was never any suggestion or desirability indicated to implant hydrogen plasma ions using PSII in order to obtain a smooth surface. Likewise, the prior art teaching the use of PSII does not suggest the desirability of using hydrogen plasma ions to create a smooth poly-Si surface morphology.

Courts have found patentable subject matter where the invention is "close on the surface" to the prior art, "but where the small difference has eluded those of ordinary skill in the art in search of the solution to a persistent problem." *In re Palmer*, 451 F.2d 1100, 1102-03, 172 USPQ 126, 128 (Fed. Cir. 1971); *citing United States v. Adams*, 383 U.S. 39, 148 USPQ 479 (1966), *Eibel Process Co. v. Minnesota & Ontario Paper Co.*, 261 U.S. 45 (1923). The present invention addresses the need for a smooth morphology with reduced surface contamination, namely metal contamination. This problem was not addressed anywhere in prior art teachings. Therefore, it could not have been obvious to one of ordinary skill in the art to combine the teachings of the prior art in order resolve the problems the present invention addresses because the prior art teachings deal with completely different issues.

The reference teachings do not suggest any desirability or motivation to combine their teachings in any manner. Nor is there any reasonable expectation of success. The Kaufman ion source implants hydrogen ions into a layer of polycrystalline silicon to provide for a thinner and smooth polycrystalline silicon film. There is no indication that the PSII would be expected by one skilled in the art to provide a successful way of implanting hydrogen ions which would provide a smooth surface morphology for a subsequently deposited polysilicon layer in a semiconductor device precursor.

While the present invention may involve some steps from each teaching, the present invention solves different problems than the problems addressed in the prior art and produces a different invention than the prior art to solve these problems. Considering that the teachings of the prior art for PSII are not applicable to the teachings of the prior

art for Kaufman ion source and the fact that the prior art and applicant solve different problems, the Examiner has used prohibited hindsight in order to combine the above mentioned reference teachings. Because the prior art does not teach or suggest the present invention, and the prior art does not express any desirability or motivation to combine their teachings, nor provide any expectation of success, the Examiner has failed to establish the necessary prima facie case for obviousness.

Claims 10-12 have been rejected under 35 USC §103(a) as being unpatentable over Burns et al. in view of applicant's admitted prior art. The Examiner asserts that Burns et al. teaches a field effect transistor having a substrate with a layer of silicon dioxide over the substrate and that the layer of silicon dioxide is covered by a layer of polycrystalline silicon, pointing to page 381 and Figure 9.8 of Burns et al. The Examiner also admits that Burns et al. does not teach implanting hydrogen ions into the silicon dioxide.

Burns et al. teaches a field effect transistor with a thin oxide layer formed so that polysilicon rows can act as an effective gate over the region. The prior art is explained above. Claim 10 recites a field effect transistor that includes "a layer of silicon dioxide having been doped with hydrogen ions deposited by a plasma source ion implantation process, wherein said layer of silicon dioxide is free of metal contamination in the layer."

Burns et al. does not teach or suggest to implant the silicon dioxide film with hydrogen ions using PSII or the need for a polycrystalline silicon layer with a smooth morphology. There is no teaching or suggestion in the prior art to create a field effect transistor using the pretreated silicon dioxide layer. Furthermore, neither the prior art nor Burns et al. teach or suggest a silicon dioxide layer which is free of metal contamination and a polycrystalline silicon layer that has a smooth morphology. Thus, claim 10 would not have been obvious.

The Examiner next rejected claim 11 pointing to pages 380-381 of Burns et al. in combination with applicant's admitted prior art. Burns et al. teaches a read-only memory

array wherein a field effect transistor is used. In the positions where a field effect transistor is desired, a thin oxide layer is formed and polysilicon rows act as an effective gate over the region the used for the field effect transistor. The prior art is explained above.

Claim 11 recites a memory array which includes "a layer of silicon dioxide that having been doped with hydrogen ions deposited by a plasma source ion implantation process, wherein said layer of silicon dioxide is free from metal contamination" and a polysilicon layer that has a smooth morphology. Burns et al. does not teach or suggest using a layer of silicon dioxide that has been implanted with hydrogen ions by PSII or the need for a smooth morphology in the polycrystalline silicon layer. Furthermore, neither the prior art nor Burns et al. teach or suggest a silicon dioxide layer which is free of metal contamination. Thus, claim 11 would not have been obvious.

The Examiner next rejects claim 12 asserting that one of ordinary skill in the art at the time of the invention would form the transistor of claim 10 or the memory array of claim 11 on a semiconductor wafer including a plurality of die. Claim 12 recites a semiconductor wafer that includes a semiconductor substrate with a layer of silicon dioxide that is formed on the semiconductor substrate and a layer of polysilicon that has a smooth morphology that is formed on the layer of silicon dioxide. The layer of silicon dioxide has been doped with hydrogen ions deposited by a PSII, wherein the layer of silicon dioxide is free from metal contamination.

One of ordinary skill in the art would not know to form the transistor of claim 10 or the memory array of claim 11. Burns et al. does not teach or suggest using a layer of silicon dioxide that has been implanted with hydrogen ions by PSII or the need for a smooth morphology in the polycrystalline layer that is also free of metal contaminates. Again, there is no teaching or suggestion in the prior art to create a field effect transistor using the pretreated silicon dioxide layer. None of the deficiencies which claim 12 cures are even mentioned or alluded to in Burns et al. Thus, claim 12 is also nonobvious.

The Examiner asserts that Burns et al. and applicant's admitted prior art are combinable because they are from the same field of endeavor. The Examiner also expresses that at the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the silicon dioxide layer. The motivation, as the Examiner claims, is to provide a layer with increased surface hardness and improved optical properties as well as avoiding metal impurities. Therefore, it is asserted by the Examiner that Burns et al. and applicant's admitted prior art are combinable to obtain the invention of claims 10-12.

Applicant respectfully disagrees that the reference teachings are combinable. The fact that the claimed invention may be within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish prima facie obviousness. MPEP §2143.01; *See also In re Lee* 61 USPQ2d 1430. Some objective reason to combine the teachings of the references must be provided. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993). The Examiner does provide a reason for motivation; however, this motivation is based on impermissible hindsight. As shown above, one skilled in the art would not know to use PSII to implant the hydrogen ions because the prior art does not teach or suggest using the same methods to obtain the same desired result as the claimed invention. Nor is there any reasonable expectation of success. Burns et al. does not solve the deficiency of the prior art. In fact Burns et al. does not even teach or suggest anything related to a smooth surface morphology with no metal contamination or the use of PSII to implant hydrogen ions. Thus, the prior art and Burns et al. cannot properly be combined to render claims 10-12 obvious.

The Examiner also rejected claim 14 under 35 USC §103(a) as being unpatentable over Murata et al (US Patent No. 5,576,229) in view of applicant's admitted prior art. The Examiner claims that Murata et al. and the prior art are combinable because they are from the same field of endeavor and that at the time of the invention it would have been obvious to a person ordinary skill in the art to implant hydrogen ions into the glass substrate. The Examiner asserts that the motivation for combining the references is to prepare the surface of the glass substrate for the deposition of a layer of polycrystalline

silicon in order to provide for a thinner and smoother polycrystalline silicon film. The Examiner further states that it would have been obvious to a person of ordinary skill in the art to implant the hydrogen atoms by PSII. The motivation is to provide a layer with increased surface hardness and improved optical properties as well as avoiding metal impurities.

Murata teaches at figure 6E a microcrystalline silicon film 502 that includes source and drain regions 507a and 507b that are doped with impurity ions. Also shown is a channel region 507 not doped with impurity ions that is formed on a substrate 501. An insulating film 503 is formed to cover the microcrystalline silicon film 502. An interlevel insulating film 508 is formed to cover the gate electrode 504. The prior art is explained above.

Applicant respectfully disagrees that the reference teachings are combinable. The fact that the claimed invention may be within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish prima facie obviousness. MPEP §2143.01. Some objective reason to combine the teachings of the references must be provided. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993). The Examiner does provide a reason for motivation; however, this motivation is based on impermissible hindsight.

Claim 14 recites a thin film transistor that includes a semiconductor substrate that is implanted with hydrogen ions and is free from metal contamination. As shown above, one skilled in the art would not know to use PSII to implant the hydrogen ions because the prior art does not teach or suggest using the same methods to obtain the same desired result as the claimed invention. Murata et al. does not solve the deficiency of the prior art. In fact Murata et al. does not even teach or suggest anything related to a smooth surface morphology with no metal contamination. Thus, the prior art and Murata et al. cannot be properly be combined to render claim 14 obvious.

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CONCLUSION

Applicants respectfully submit that, in view of the above remarks, the application is now in condition for allowance. Early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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